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January 20177

# FUSB252 Type-C CC with High Speed Digital (HSD) Port Protection Switch

## Features

- Fully Type-C Port Protection
- Supports USB Type-C™ Specification 1.2
- $V_{CC}$  0 V- 5.5 V
- 20 V DC Protection on  $V_{CC}$
- 16 V DC protection on HSD Port
- $V_{DD}$  Operating Range, 2.7 V- 5.5 V
- Current Capability: 1 A
- CC  $R_{ON}$ : 0.3  $\Omega$  Typical
- HSD  $R_{ON}$ : 5  $\Omega$  Typical
- Wide -3 db Bandwidth: 1 GHz
- Low Power Operation:  $I_{CC}$  = 9  $\mu$ A Typical
- Dead Battery Support (UFP Support when No Power Applied)
- CC Over-Voltage Protection: Typical = 5.6 V

## Description

The FUSB252 is an integrated port protection switch for USB Type-C applications. This product will protect HSD+/- and CCx pins when stressed with voltages up to 20 V. Over-Voltage Protection (OVP) at 5.8 V typical will protect the system for Electrical Overstress (EOS) damage. With a fully integrated USB 2.0 switch for HSD+/-, this product can be easily integrated into existing solutions. The HSD switches can pass USB 2.0 signals with bandwidth 1 GHz to maintain signal integrity and eye compliance.

The CC switches have very low  $R_{ON}$  of 0.3  $\Omega$  to minimize signal attenuation. The FUSB252 also provides Dead Battery support per the Type-C specification. Additional features include Under-Voltage Lockout (UVLO) and thermal shutdown.

## Applications

- Smartphones
- Tablets
- Laptops

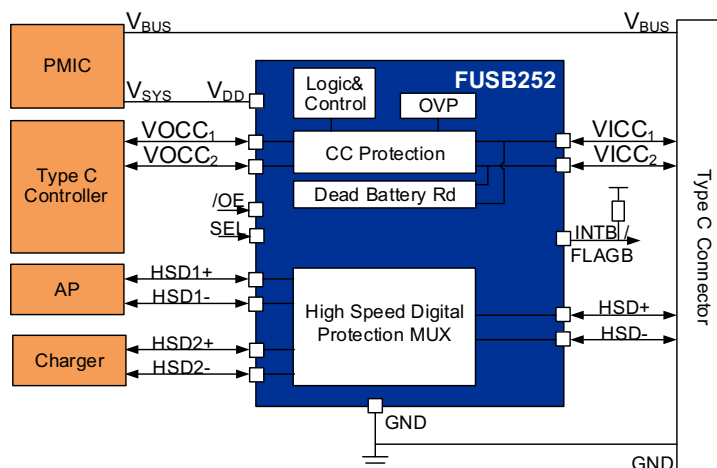


Figure 1. Typical Application

## Ordering Information

| Part Number | Operating Temperature Range | Package                                                       | Packing Method | Top Mark |
|-------------|-----------------------------|---------------------------------------------------------------|----------------|----------|
| FUSB252UMX  | -40 to 85°C                 | 16-Lead Ultrathin Molded Leadless Package (UMLP) 1.8 x 2.6 mm | Tape and Reel  | UZ       |

USB Type-C™ is a trademark of USB Implementers Forum, Inc.

## Block Diagram

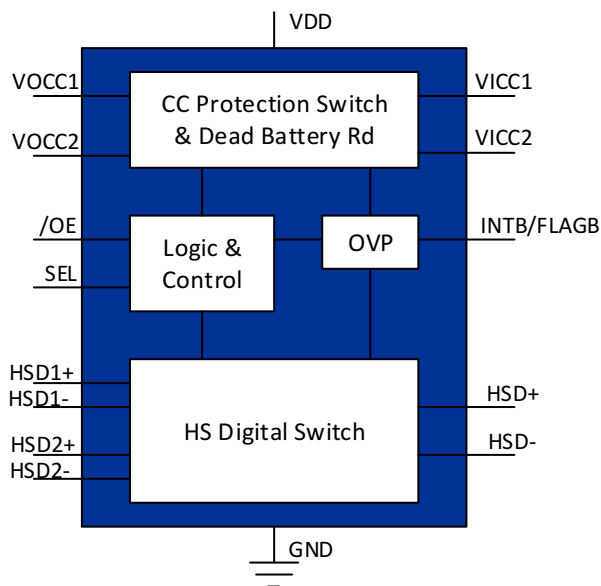


Figure 2. Block Diagram

## Reference Schematic

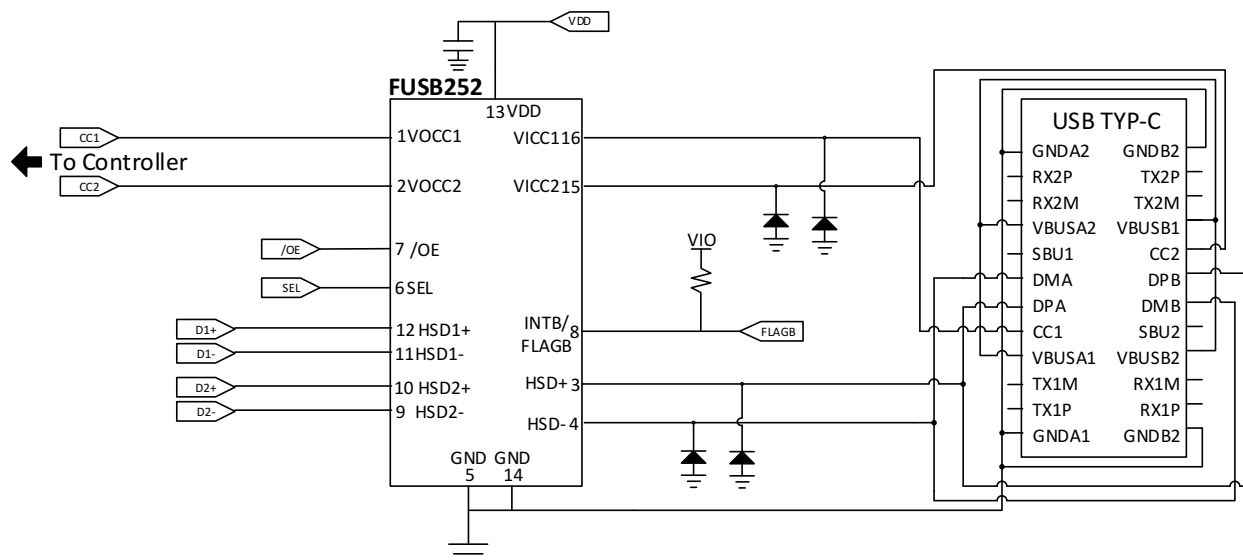


Figure 3. Reference Schematic

## Pin Configuration

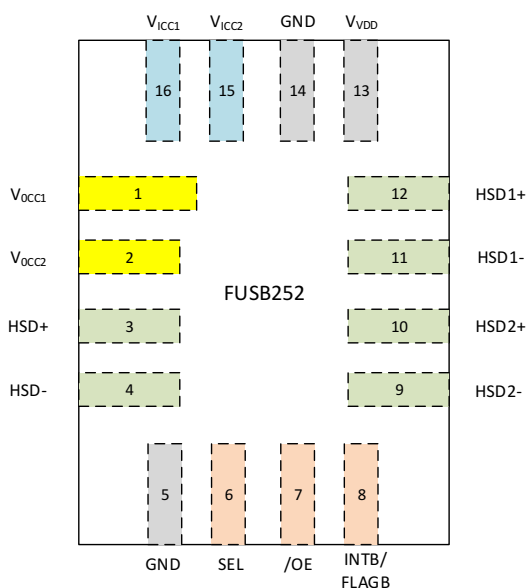


Figure 4. Pin Assignment (Top Through View)

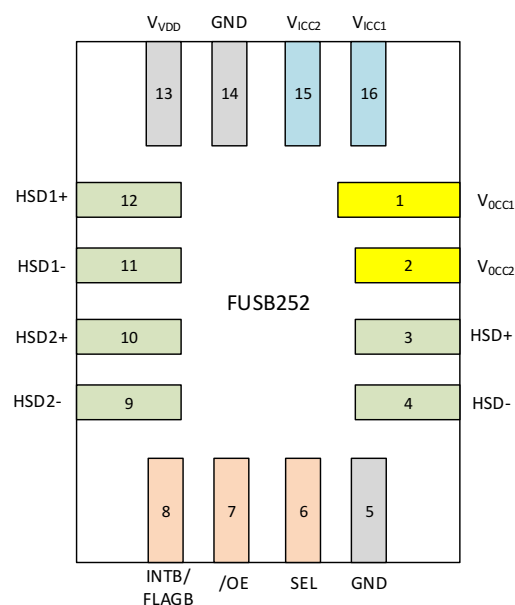


Figure 5. Pin Assignment (Bottom View)

## Pin Descriptions

| Bump                                         | Name       | Type   | Description                                                    |
|----------------------------------------------|------------|--------|----------------------------------------------------------------|
| <b>Power Interface</b>                       |            |        |                                                                |
| 13                                           | VDD        | Power  | Power                                                          |
| 5,14                                         | GND        | Ground | Ground                                                         |
| <b>USB Type-C Connector Interface Input</b>  |            |        |                                                                |
| 15, 16                                       | VICC1,2    | Input  | Type C CC Interface OVP protection input, Connect to connector |
| <b>USB Type-C Connector Interface Output</b> |            |        |                                                                |
| 1, 2                                         | VOCC1,2    | Output | Type C CC Interface output. Connect to controller              |
| <b>USB High Speed Data Interface</b>         |            |        |                                                                |
| 3                                            | HSD+       | I/O    | Common High Speed Digital / USB Data Bus                       |
| 4                                            | HSD-       | I/O    | Common High Speed Digital / USB Data Bus                       |
| 12                                           | HSD1+      | I/O    | Multiplexed Source Input 1                                     |
| 11                                           | HSD1-      | I/O    | Multiplexed Source Input 1                                     |
| 10                                           | HSD2+      | I/O    | Multiplexed Source Input 2                                     |
| 9                                            | HSD2-      | I/O    | Multiplexed Source Input 2                                     |
| <b>Signal Interface</b>                      |            |        |                                                                |
| 7                                            | /OE        | I/O    | Switch Enable                                                  |
| 6                                            | SEL        | I/O    | Switch Select                                                  |
| 8                                            | INTB/FLAGB | Output | OVP Interrupt Flag                                             |

**Table 1. CC Switch Truth Table Configuration**

| $V_{DD}$               | $V_{ICC}$ Voltage | CC Switch Configuration      |
|------------------------|-------------------|------------------------------|
| 0 V - UVLO (Not Valid) | 0 V – 5.8 V       | OFF Dead Battery Rd Inserted |
|                        | 5.8 V to 20 V     | OFF Dead Battery Rd Inserted |
| 2.7 V – 5.5 V (Valid)  | 0 V – 5.8 V       | On                           |
|                        | 5.8 V to 20 V     | OFF (OVP)                    |

**Table 2. Device Truth Table Configuration**

| /OE | SEL | VDD       | HSD+/HSD-       | CC           |
|-----|-----|-----------|-----------------|--------------|
| 1   | 0   | Not Valid | X (Open/High-Z) | Dead Battery |
| 0   | 0   | Not Valid | X (Open/High-Z) | Dead Battery |
| 1   | X   | Valid     | X (Open/High-Z) | On           |
| 0   | 0   | Valid     | HSD1+/HSD1-     | On           |
| 0   | 1   | Valid     | HSD2+/HSD2-     | On           |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol                             | Parameter                                       |                                                                                |         | Min. | Max.             | Unit |
|------------------------------------|-------------------------------------------------|--------------------------------------------------------------------------------|---------|------|------------------|------|
| V <sub>VDD</sub>                   | Supply Voltage from V <sub>DD</sub>             |                                                                                |         | -0.5 | 12.0             | V    |
| V <sub>VICC</sub>                  | V <sub>ICC</sub> x, to GND                      |                                                                                |         | -0.5 | 24               | V    |
| V <sub>SW</sub>                    | V <sub>HSD</sub> ±, to GND                      |                                                                                |         | -5   | 16               | V    |
| V <sub>OCC</sub> , V <sub>SW</sub> | V <sub>OCC</sub> x V <sub>HSD</sub> x+/- to GND |                                                                                |         | -0.5 | 6                | V    |
| V <sub>CONTROL</sub>               | DC Input Voltage (S, /OE)                       |                                                                                |         | -0.5 | V <sub>VDD</sub> | V    |
| I <sub>CCSW</sub>                  | DC CC Switch Current                            |                                                                                |         |      | 1.25             | A    |
| I <sub>USBSW</sub>                 | DC Output Current                               |                                                                                |         |      | 100              | mA   |
| I <sub>IK</sub>                    | DC Input Diode Current                          |                                                                                |         | -50  |                  | mA   |
| T <sub>STORAGE</sub>               | Storage Temperature Range                       |                                                                                |         | -65  | +150             | C    |
| T <sub>J</sub>                     | Maximum Junction Temperature                    |                                                                                |         |      | +150             | C    |
| T <sub>L</sub>                     | Lead Temperature (Soldering, 10 seconds)        |                                                                                |         |      | +260             | C    |
| ESD                                | IEC 61000-4-2 System ESD                        | Connector Pins<br>(V <sub>VDD</sub> , V <sub>ICC</sub> x, V <sub>HSD</sub> ±,) | Air Gap | 15   |                  | kV   |
|                                    |                                                 |                                                                                | Contact | 8    |                  |      |
|                                    | IEC 61000-4-5 Surge ESD                         | V <sub>ICC</sub> x to GND                                                      |         | -24  | 24               | V    |
|                                    |                                                 | V <sub>HSD</sub> ± to GND                                                      |         | -16  | 16               | V    |
|                                    | Human Body Model, JEDEC JESD22-A114             | Power to GND                                                                   |         | 4    |                  | kV   |
|                                    |                                                 | External Pins to GND<br>(V <sub>HSD</sub> ±, V <sub>ICC</sub> x)               |         |      |                  |      |
|                                    |                                                 | System Side Pin<br>(V <sub>HSD</sub> x±, V <sub>OCC</sub> x, S, /OE, FLAGB)    |         | 2    |                  |      |
|                                    | Charged Device Model, JEDEC LESD22-C101         | All Pins                                                                       |         | 1    |                  |      |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. ON does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol      | Parameter                        | Min. | Typ. | Max.     | Unit |
|-------------|----------------------------------|------|------|----------|------|
| $V_{DD}$    | Supply Voltage                   | 2.7  | 4.2  | 5.5      | V    |
| $V_{ICC}$   | Type C Input Voltage             | 0    |      | 5.5      | V    |
| $V_{OCC}$   | Type C Output Voltage            | 0    |      | 5.5      | V    |
| $I_{CCSW}$  | Maximum CC Switch Current        |      |      | 1        | A    |
| $V_{CNTRL}$ | Control Input Voltage (SEL, /OE) | -0.5 |      | $V_{DD}$ | V    |
| $V_{SW}$    | HSD/USB Switch I/O Voltage       | -0.5 |      | 4.5      | V    |
| $T_A$       | Operating Temperature            | -40  |      | +85      | C    |

## DC Electrical Characteristics

Unless otherwise specified: Recommended  $T_A$  and  $T_J$  temperature ranges. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{DD}=4.2\text{ V}$  unless otherwise specified.

| Symbol                     | Parameter                         | V <sub>DD</sub> (V) | Conditions                                       | T <sub>A</sub> = -40 to +85°C<br>T <sub>J</sub> = -40 to +125°C |      |      | Unit |
|----------------------------|-----------------------------------|---------------------|--------------------------------------------------|-----------------------------------------------------------------|------|------|------|
|                            |                                   |                     |                                                  | Min.                                                            | Typ. | Max. |      |
| Basic Operation Device     |                                   |                     |                                                  |                                                                 |      |      |      |
| I <sub>CC</sub>            | Quiescent Supply Current          | 2.7 to 5.5          | /OE = L, I <sub>OUT</sub> =0                     |                                                                 | 9    |      | μA   |
|                            |                                   |                     | /OE = H I <sub>OUT</sub> =0                      |                                                                 | 9    |      |      |
| I <sub>OFF</sub>           | Power-Off Leakage Current         | 0                   |                                                  |                                                                 | 3    |      | μA   |
| Basic Operation CC switch  |                                   |                     |                                                  |                                                                 |      |      |      |
| I <sub>SD(DB)</sub>        | Dead Battery Supply Current       | 0 to UVLO           | Dead Battery State Supply Current                |                                                                 | 15   |      | uA   |
| R <sub>ON</sub>            | CC Path On Resistance             | 2.7 to 5.5          | I <sub>OUT</sub> = 200 mA                        |                                                                 | 350  | 480  | mΩ   |
| V <sub>OV_TRIP</sub>       | Input OVP Lockout                 | 2.7 to 5.5          | V <sub>ICC</sub> Rising                          |                                                                 | 5.65 | 6.20 | V    |
|                            |                                   |                     | V <sub>ICC</sub> Falling                         |                                                                 | 5.3  |      |      |
| V <sub>OV_HYS</sub>        | Input OVP Hysteresis              | 2.7 to 5.5          |                                                  |                                                                 | 0.35 |      | V    |
| V <sub>UVLO</sub>          | Under-Voltage Lockout             | 2.7 to 5.5          | V <sub>DD</sub> Rising                           |                                                                 | 2.55 | 2.70 | V    |
|                            |                                   |                     | V <sub>DD</sub> Falling                          |                                                                 | 2.5  |      |      |
| TSD                        | Thermal Shutdown <sup>(1)</sup>   |                     | Shutdown Threshold                               |                                                                 | 150  |      | °C   |
|                            |                                   |                     | Return from Shutdown                             |                                                                 | 130  |      |      |
|                            |                                   |                     | Hysteresis                                       |                                                                 | 20   |      |      |
| R <sub>d</sub>             | Dead Battery Pull-Down Resistance | 0 to UVLO           | Dead Battery Resistance                          | 4.08                                                            | 5.10 | 6.12 | kΩ   |
|                            |                                   |                     | Voltage on Pin                                   | 0.25                                                            |      | 2.6  | V    |
| Basic Operation HSD Switch |                                   |                     |                                                  |                                                                 |      |      |      |
| V <sub>OV_TRIP</sub>       | Input OVP Lockout                 | 2.7 to 5.5          | V <sub>HSD±</sub> Rising                         |                                                                 | 4.4  | 5.0  | V    |
|                            |                                   |                     | V <sub>HSD±</sub> Falling                        |                                                                 | 4.1  |      |      |
| V <sub>OV_HYS</sub>        | Input OVP Hysteresis              | 2.7 to 5.5          |                                                  |                                                                 | 0.3  |      | V    |
| V <sub>UV_TRIP</sub>       | Input Under-Voltage Lockout       | 2.7 to 5.5          |                                                  |                                                                 | -1.2 |      | V    |
| V <sub>IH</sub>            | Input Voltage High                | 2.7 to 5.5          |                                                  | 1.3                                                             |      |      | V    |
| V <sub>IL</sub>            | Input Voltage Low                 | 2.7 to 5.5          |                                                  |                                                                 |      | 0.5  | V    |
| I <sub>IN</sub>            | Control Input Leakage             | 2.7 to 5.5          | V <sub>SW</sub> = 0 to V <sub>DD</sub>           |                                                                 | 0.1  |      | μA   |
| I <sub>OZ</sub>            | Off State Leakage                 | 4.2                 | 0≤HSDn ≤3.6 V                                    |                                                                 | 2    |      | μA   |
|                            |                                   | 4.2                 | 0≤HSD1n <sub>±</sub> , HSD2n <sub>±</sub> ≤3.6 V |                                                                 | 100  |      | nA   |
| R <sub>ON</sub>            | HS Switch On Resistance           | 4.2                 | V <sub>SW</sub> = 0.4 V, I <sub>ON</sub> = -8 mA |                                                                 | 5    |      | Ω    |
| ΔR <sub>ON</sub>           | HS Delta R <sub>ON</sub>          | 4.2                 | V <sub>SW</sub> = 0.4 V, I <sub>ON</sub> = -8 mA |                                                                 | 0.1  |      | Ω    |

**Note:**

- Guaranteed by characterization, not production tested

## AC Electrical Characteristics

Unless otherwise specified: Recommended  $T_A$  and  $T_J$  temperature ranges. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{DD}=3.8\text{ V}$  unless otherwise specified.

| Symbol                      | Parameter                                                            | V <sub>DD</sub> (V) | Conditions                                                                                                                                   | T <sub>A</sub> = -40 to +85°C<br>T <sub>J</sub> =-40 to +125°C |      |      | Unit |
|-----------------------------|----------------------------------------------------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|------|------|------|
|                             |                                                                      |                     |                                                                                                                                              | Min.                                                           | Typ. | Max. |      |
| CC Switch Timing Parameter  |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| t <sub>OVP</sub>            | Response Time <sup>(2)</sup>                                         | 2.7 to 5.5          | I <sub>OUT</sub> = 0.2 A, C <sub>L</sub> = 200 pF,<br>V <sub>ICCX</sub> 5 V to 6 V                                                           |                                                                | 0.5  | 1.0  | μs   |
| t <sub>ON</sub>             | Turn-On Time                                                         |                     | VDD Rising 2 V to 3 V                                                                                                                        |                                                                | 25   |      | ms   |
| T <sub>MBB</sub>            | Make-Before-Break                                                    | 2.7 to 5.5          | VDD Rising 2 V to 3 V                                                                                                                        |                                                                | 600  |      | ns   |
| CC Switch Capacitance       |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| C <sub>ON</sub>             | Switch Path On Capacitance <sup>(2)</sup>                            | 2.7 to 5.5          |                                                                                                                                              |                                                                | 100  |      | pF   |
| CC Switch Bandwidth         |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| BW                          | PD Traffic Bandwidth <sup>(2)</sup>                                  | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 200 pF                                                                                               |                                                                | 25   |      | MHz  |
| HSD Switch Timing Parameter |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| t <sub>OVP</sub>            | Response Time <sup>(2)</sup>                                         | 2.7 to 5.5          | I <sub>OUT</sub> = 0.2 A, V <sub>D±</sub> 4 V to 5 V                                                                                         |                                                                | 0.5  | 1.0  | μs   |
| t <sub>ON</sub>             | Turn-On Time, /OE to Output <sup>(2)</sup>                           | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF,<br>V <sub>SW</sub> = 0.8 V                                                                     |                                                                | 25   |      | ms   |
| t <sub>OFF</sub>            | Turn-Off Time, /OE to Output <sup>(2)</sup>                          | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF,<br>V <sub>SW</sub> = 0.8 V                                                                     |                                                                | 100  | 400  | ns   |
| t <sub>PD</sub>             | Propagation Delay <sup>(2)</sup>                                     | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF,                                                                                                |                                                                | 0.25 |      | ns   |
| T <sub>BBM</sub>            | Break-Before-Make <sup>(2)</sup>                                     | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF,<br>V <sub>SWx</sub> = 0.8 V SEL= H <-> L                                                       |                                                                | 100  |      | μs   |
| O <sub>IRR</sub>            | Off Isolation                                                        | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, f = 240 MHZ                                                                                                           |                                                                | -25  |      | dB   |
| Xtalk                       | Non-Adjacent Channel Crosstalk                                       | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, f = 240 MHZ                                                                                                           |                                                                | -40  |      | dB   |
| HSD Switch Capacitance      |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| C <sub>IN</sub>             | Control Pin Input Capacitance <sup>(2)</sup>                         | 0                   |                                                                                                                                              |                                                                | 1.5  |      | pF   |
| C <sub>ON</sub>             | HSD+/HSD- On Capacitance <sup>(2)</sup>                              | 2.7 to 5.5          | /OE = L, f = 240 MHz,                                                                                                                        |                                                                | 4    |      |      |
| C <sub>OFF</sub>            | HSD1 <sub>x</sub> , HSD2 <sub>x</sub> Off Capacitance <sup>(2)</sup> | 2.7 to 5.5          | /OE = H                                                                                                                                      |                                                                | 2.5  |      |      |
| USB Switch Bandwidth        |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| BW                          | -3 db Bandwidth <sup>(2)</sup>                                       | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF                                                                                                 |                                                                | 1400 |      | MHz  |
|                             |                                                                      | 2.7 to 5.5          | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF                                                                                                 |                                                                | 560  |      |      |
| USB High-Speed-Related      |                                                                      |                     |                                                                                                                                              |                                                                |      |      |      |
| t <sub>SK(P)</sub>          | Skew of Opposite Transitions of the Same Output <sup>(2)</sup>       |                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5pF                                                                                                  |                                                                | 25   |      | ps   |
| t <sub>J</sub>              | Total Jitter <sup>(2)</sup>                                          |                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF,<br>t <sub>R</sub> = t <sub>F</sub> = 500 ps (10-90%) at<br>480 Mbps (PRBS=2 <sup>15</sup> – 1) |                                                                | 200  |      | ps   |

### Note:

- Guaranteed by characterization, not production tested.



## Operation and Application Description

### Out of Spec Surge/Spike Voltage due to Hot Plug

The FUSB252 protects end systems against 20 V DC on the CC pin, in cases where the FUSB252 is tested to mimic a hot plug event, a fully charged cable connected to a power supply set to 20 V is used to zap the VICC pins of the device. In these cases, the inductance of the cable causes voltage spikes that are higher than the absolute maximum ratings of the of the VICC pins. These voltages can cause damage to the VOCC pins. This scenario does not occur in normal usage. The Type-C specification prevents the plug from having 20V on VBUS from a PD source prior to a PD contract being completed. When the 20 V potential is on VBUS and shorted to the CC pin, it causes a detach and the voltage spikes are less likely to occur. The following reference circuit is required when the application calls for additional protection to protect against such event as hot plug.

### Application Specific Schematic

- Place a 5 V to 6 V rated Zener TVS diode such as (CZRF52C5V6 or CD1005-Z5V1) on the VOCC pin, and a 5  $\Omega$  resistor to device ground to prevent the FUSB252 from being damaged during these tests. With this additional protection if is also important to select the right external VICC IEC TVS for the best overall performance.
- Without the additional protection the device by itself can withstand up to 9 V under the same hot plug condition

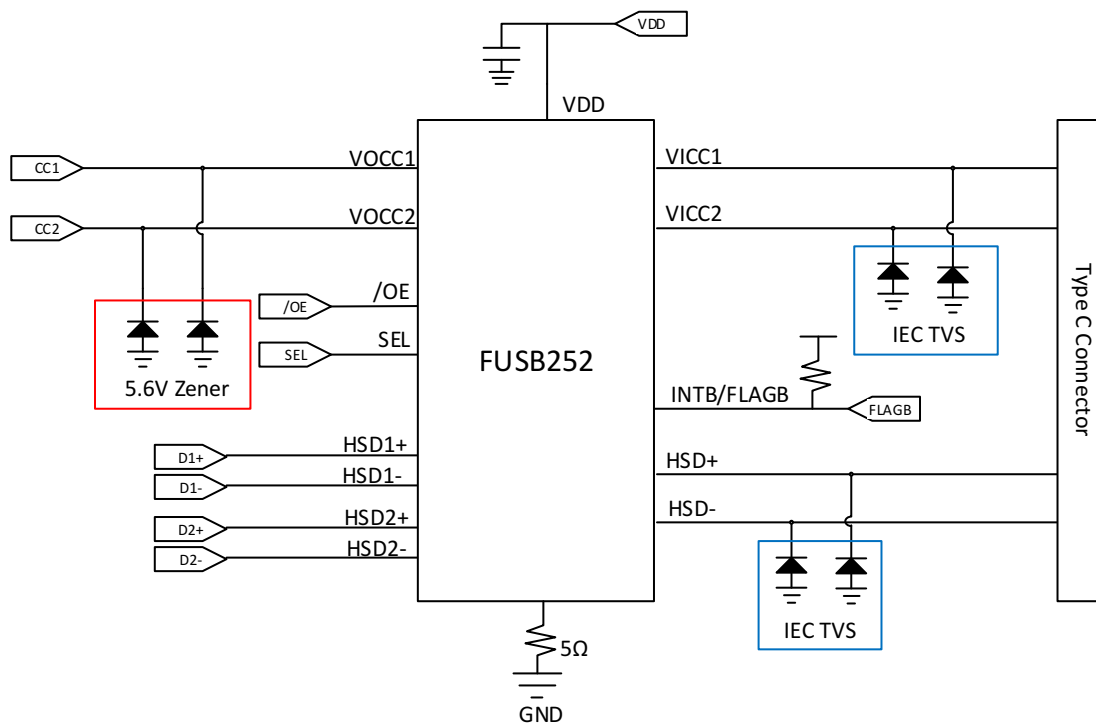


Figure 6. Reference Schematic

### Over-Voltage Protection

When over-voltage event is detected, device will activate OVP to shutdown the switch within  $t_{OVP}$ , as well as signal the FLAGB to indicate there is OV event to the system.

### Fault Reporting

Upon the detection of an over-voltage event, the INTB/FLAGB signals the fault by activating LOW.

## Type-C Solution Reference

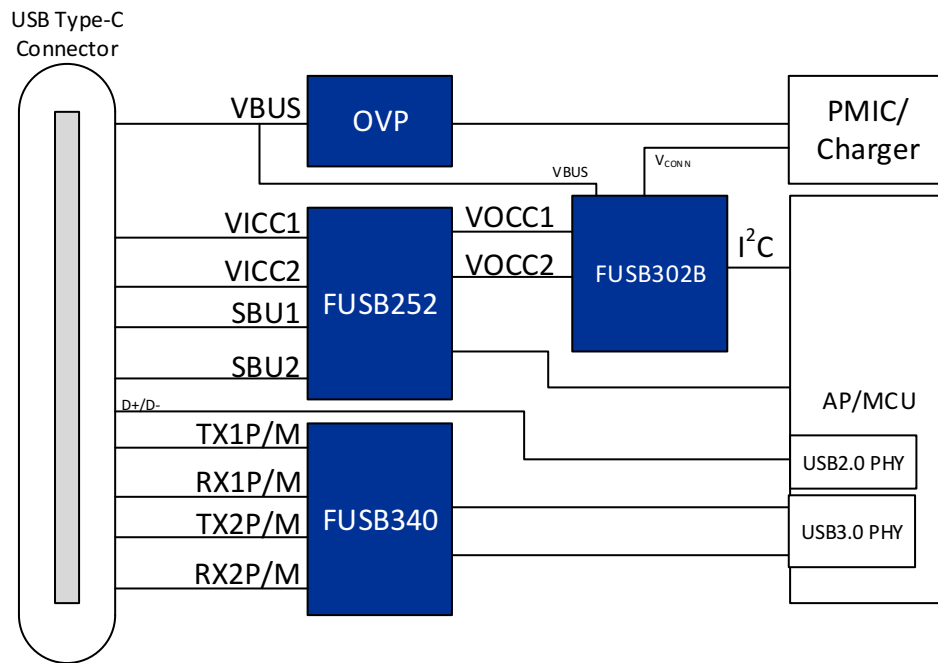


Figure 7. Example of Type-C Solution Reference (SBU)

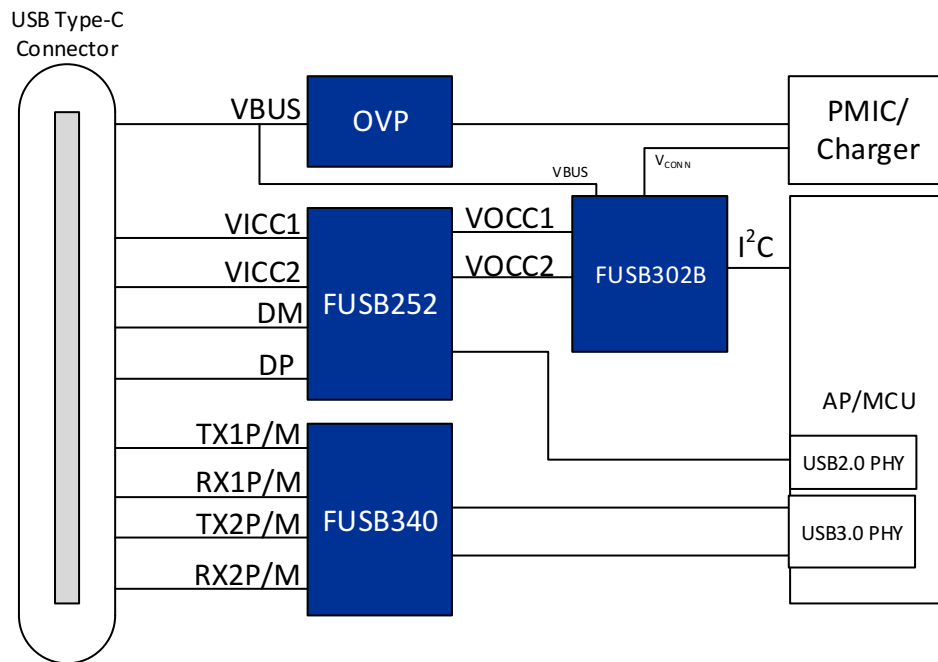


Figure 8. Example of Type-C Solution Reference (USB)

## Test Diagrams

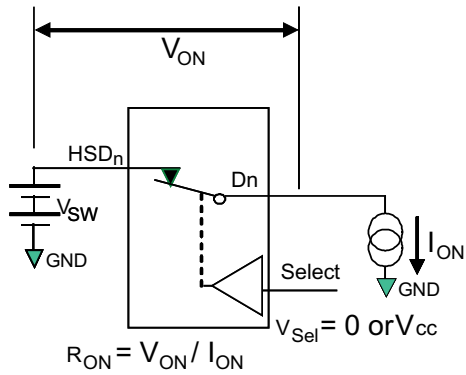
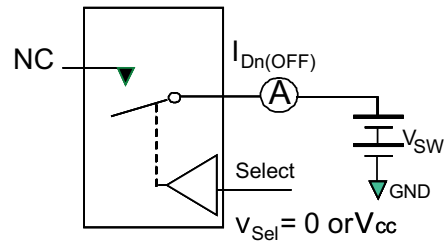
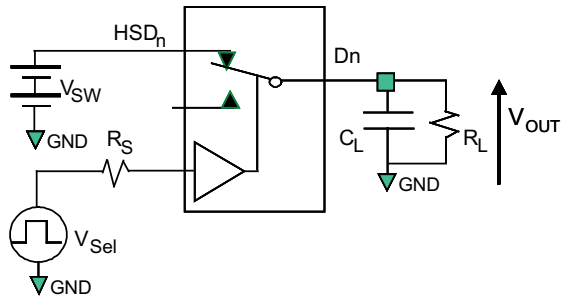


Figure 9. On Resistance



\*\*Each switch port is tested separately

Figure 10. Off Leakage



$R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC Tables for specific values)  
 $C_L$  includes test fixture and stray capacitance.

Figure 11. AC Test Circuit Load

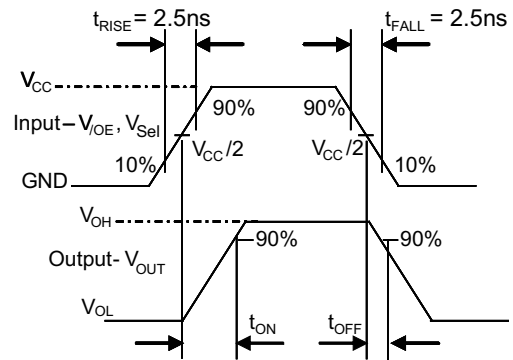


Figure 12. Turn-On / Turn-Off Waveforms

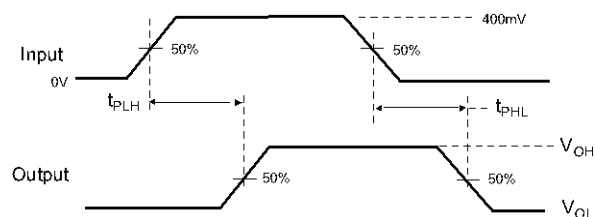


Figure 13. Propagation Delay ( $t_{rtF} - 500 \text{ ps}$ )

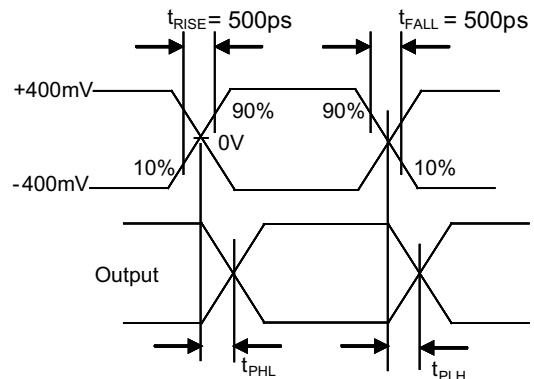


Figure 14. Intra-Pair Skew Test  $t_{SK(P)}$

## Test Diagrams (Continued)

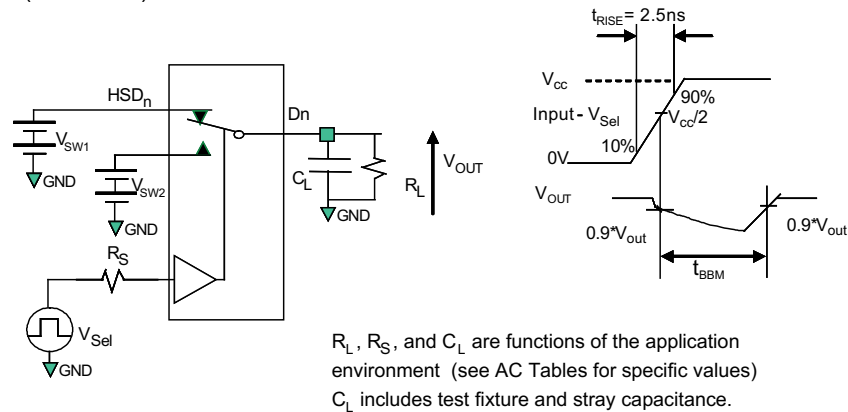


Figure 15. Break-Before-Make Interval Timing

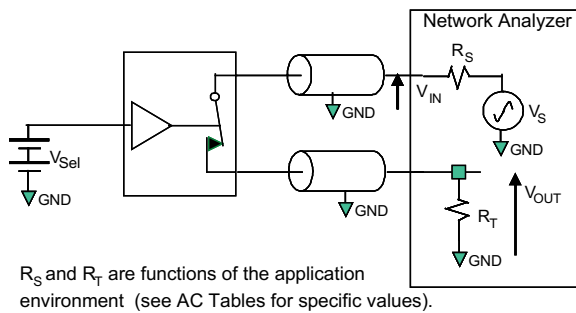


Figure 16. Bandwidth

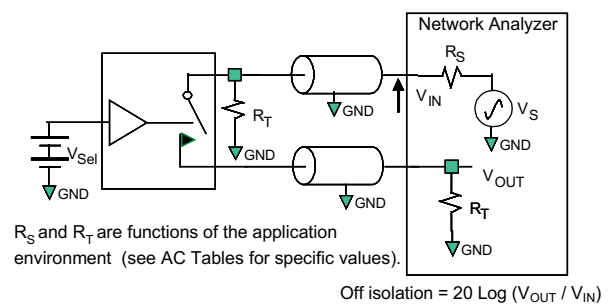


Figure 17. Channel Off Isolation

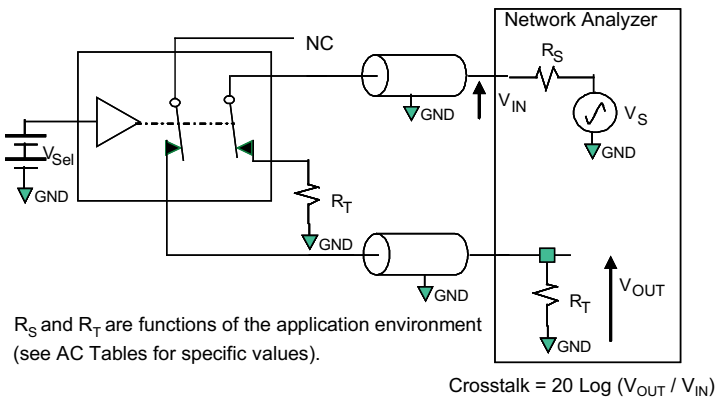


Figure 18. Non-Adjacent Channel-to-Channel Crosstalk

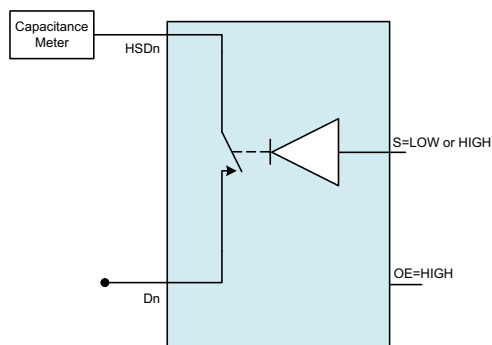


Figure 19. Channel Off Capacitance

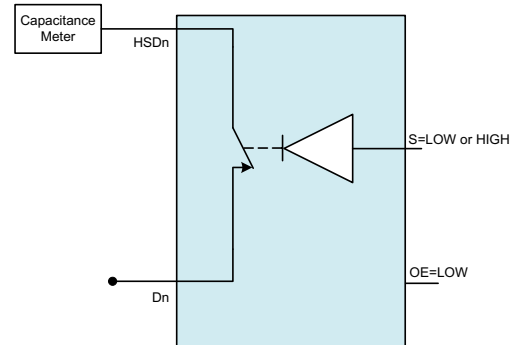
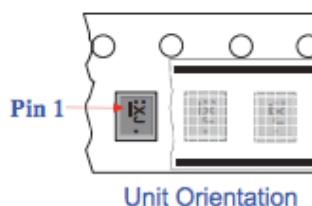
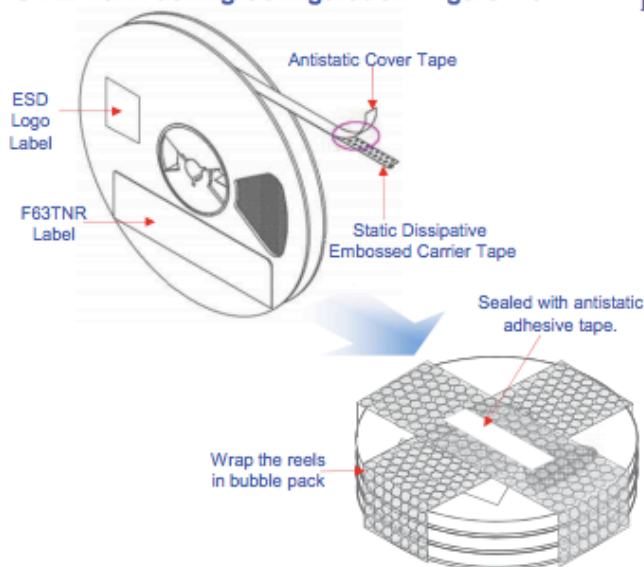


Figure 20. Channel On Capacitance

## Package Information

**UMLP16A Packing Configuration: Figure 1.0**



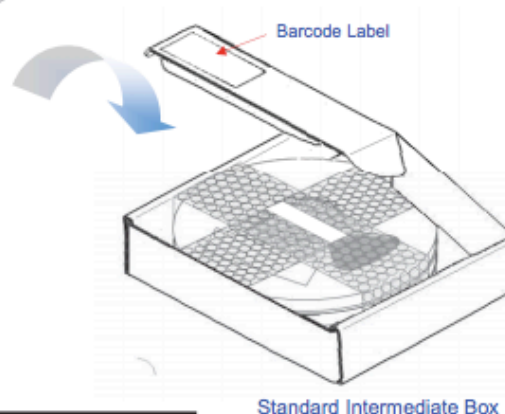
**Packaging Description:**

UMLP16 pins products are classified under Moisture Sensitive Level 1 at 260°C peak package body temperature.

The carrier tape is made from dissipative polystyrene or polycarbonate resin. The cover tape is a multilayer film primarily composed of polyester film, adhesive layer, heat activated sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 5000 units per 178 mm diameter reel. Up to three reels are packed in each intermediate box. The reels is made of polystyrene plastic (anti-static coated or intrinsic).

These full reels are individually barcode labeled and placed inside a pizza box made of recyclable corrugated brown paper with a Fairchild logo printing. These pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

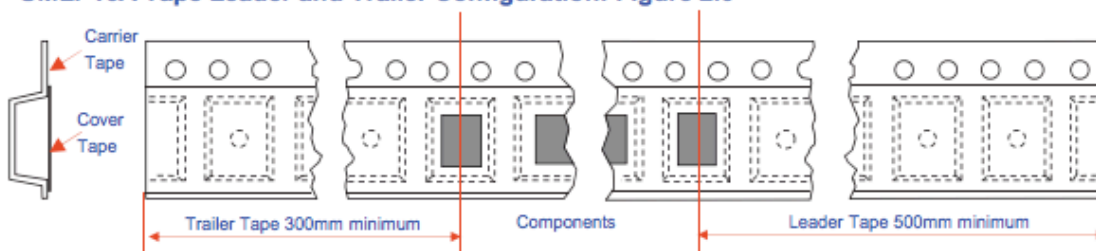
| UMLP16A Packing Information |                         |
|-----------------------------|-------------------------|
| Packaging Option            | Standard (no flow code) |
| Packaging type              | TNR                     |
| Qty per Reel                | 5000                    |
| Reel Size                   | 7" Dia                  |
| Box Dimension (mm)          | 193X183X80              |
| Max qty per Box             | 15,000                  |



**F63TNR Label Sample**

|                     |                                       |
|---------------------|---------------------------------------|
| LOT: PMH01008888    | QTY: 5000                             |
| FSID: FXLA104QFX    | SPEC:                                 |
| D/C1: P1323AF QTY1: | SPEC REV: 2nd Level Interconnect      |
| D/C2: QTY2:         | 1. Category G3                        |
| Green Component     | 2. Maximum safe temperature 260 deg C |
| RoHS COMPLIANT      | 3. MSL 1                              |
|                     | FAIRCHILD SEMICONDUCTOR               |

**UMLP16A Tape Leader and Trailer Configuration: Figure 2.0**

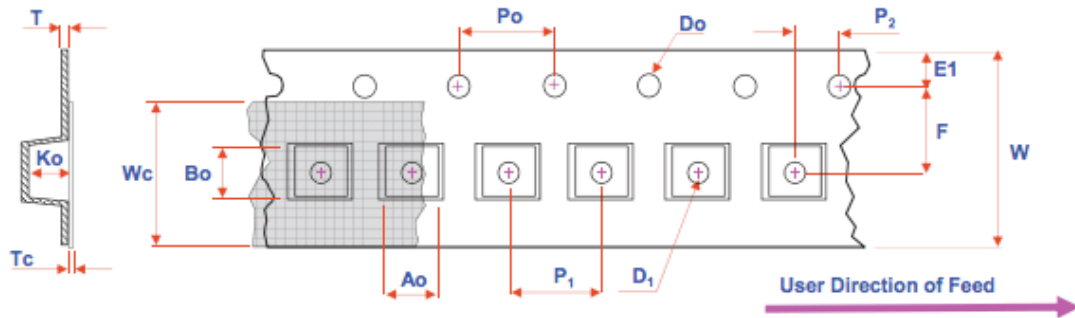


**NOTES:**

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

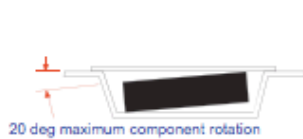
B : DRAWING FILE NAME : PKG-UMLP16AREV2

Embossed Carrier Tape Configuration: Figure 3.0

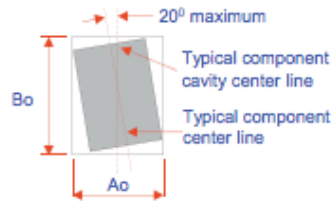


| Dimensions are in millimeters |             |             |             |           |             |            |             |           |           |             |          |              |            |           |
|-------------------------------|-------------|-------------|-------------|-----------|-------------|------------|-------------|-----------|-----------|-------------|----------|--------------|------------|-----------|
| Package                       | Ao<br>±0.05 | Bo<br>±0.05 | Do<br>±0.10 | D1<br>Min | E1<br>±0.10 | F<br>±0.10 | Ko<br>±0.05 | P1<br>TYP | Po<br>TYP | P2<br>±0.05 | T<br>TYP | Tc<br>±0.005 | W<br>±0.30 | Wc<br>TYP |
| UMLP1.8x2.6                   | 2.00        | 2.80        | 1.50        | 0.6       | 1.75        | 3.5        | 0.70        | 4.0       | 4.0       | 2.0         | 0.254    | 0.06         | 8.0        | 5.3       |

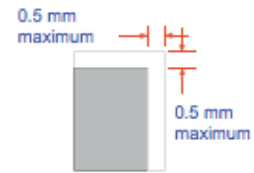
Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA /Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)  
Component Rotation

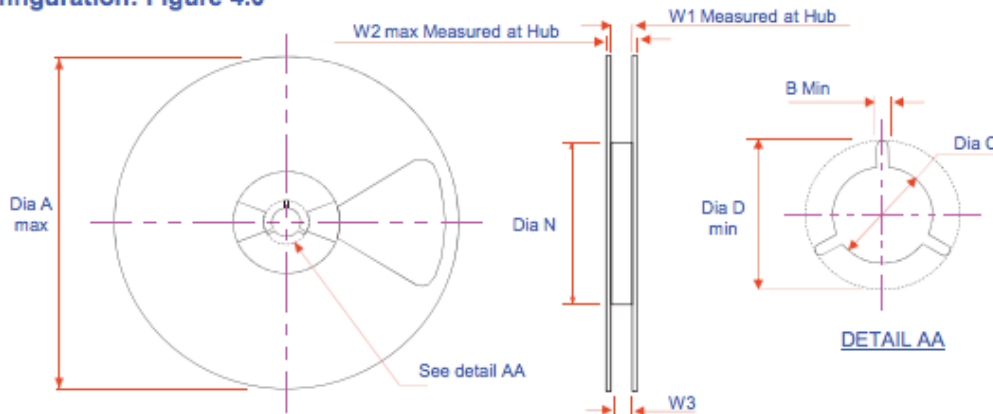


Sketch B (Top View)  
Component Rotation



Sketch C (Top View)  
Component lateral movement

Reel Configuration: Figure 4.0

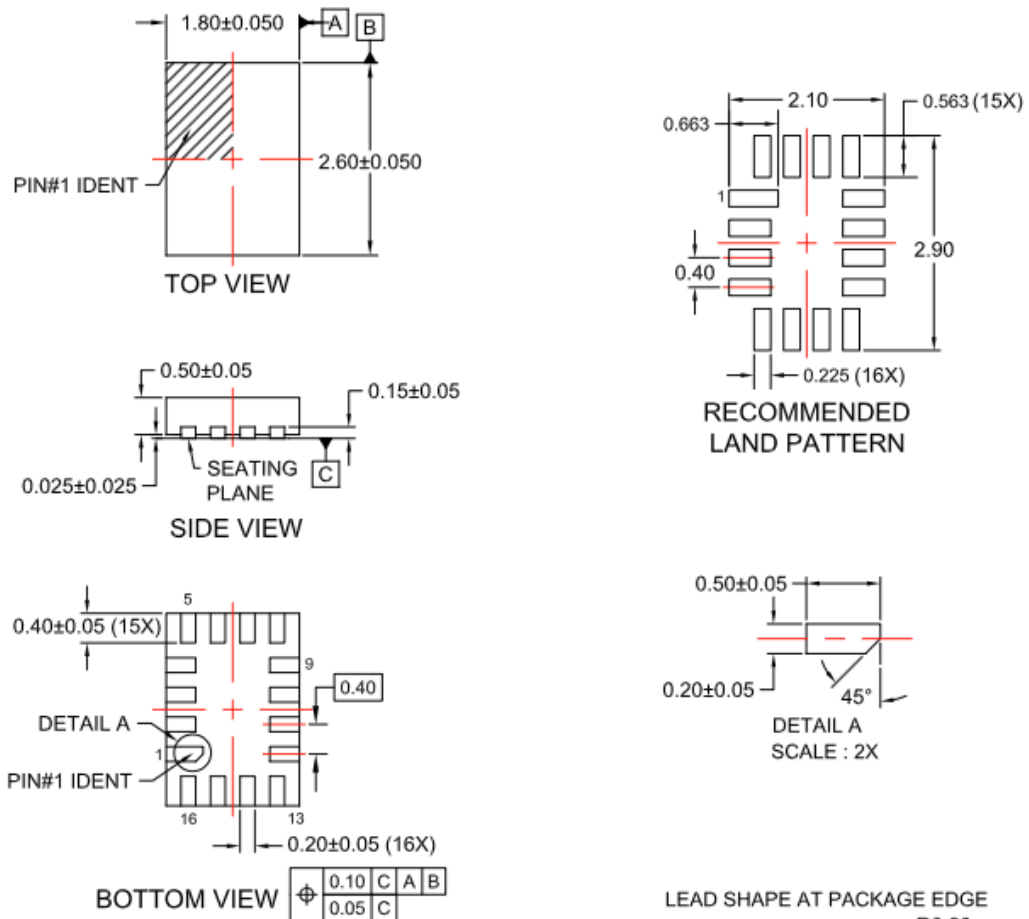


| Dimensions are in millimeters |             |           |           |                 |           |           |              |            |                  |
|-------------------------------|-------------|-----------|-----------|-----------------|-----------|-----------|--------------|------------|------------------|
| Tape Width                    | Reel Option | Dia A max | Dia B min | Dia C +0.5/-0.2 | Dia D min | Dim N min | Dim W1 ±2/-0 | Dim W2 Max | Dim W3 (LSL-USL) |
| 8 mm                          | 7" Dia      | 178.0     | 1.5       | 13.0            | 20.2      | 55.0      | 8.4          | 14.4       | 7.9~10.9         |

NOTES:

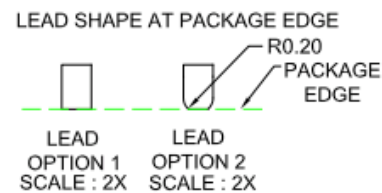
- A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
- B : DRAWING FILE NAME : PKG-UMLP16AREV2
- C : PLASTIC REEL W1 DIMENSION CONTROL LIMIT OF:  
8MM REEL=±1.0MM AND 12MM REEL AND ABOVE =±1.5MM

## Physical Dimensions



### NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-UMLP16ArevF.
- F. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.



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**Figure 21. 16 Lead, UMLP, 0.55 mm x 1.8 mm x 2.6 mm**

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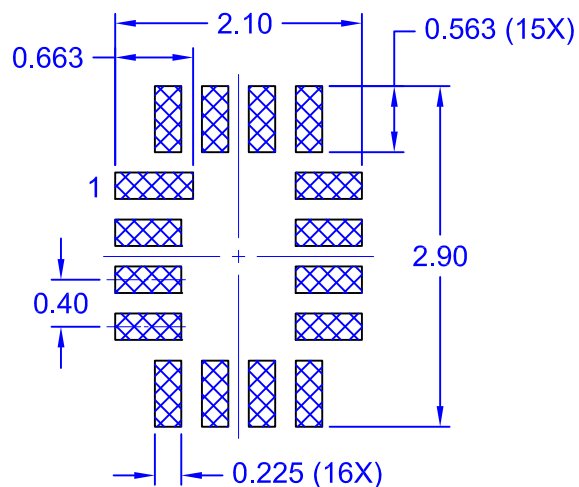
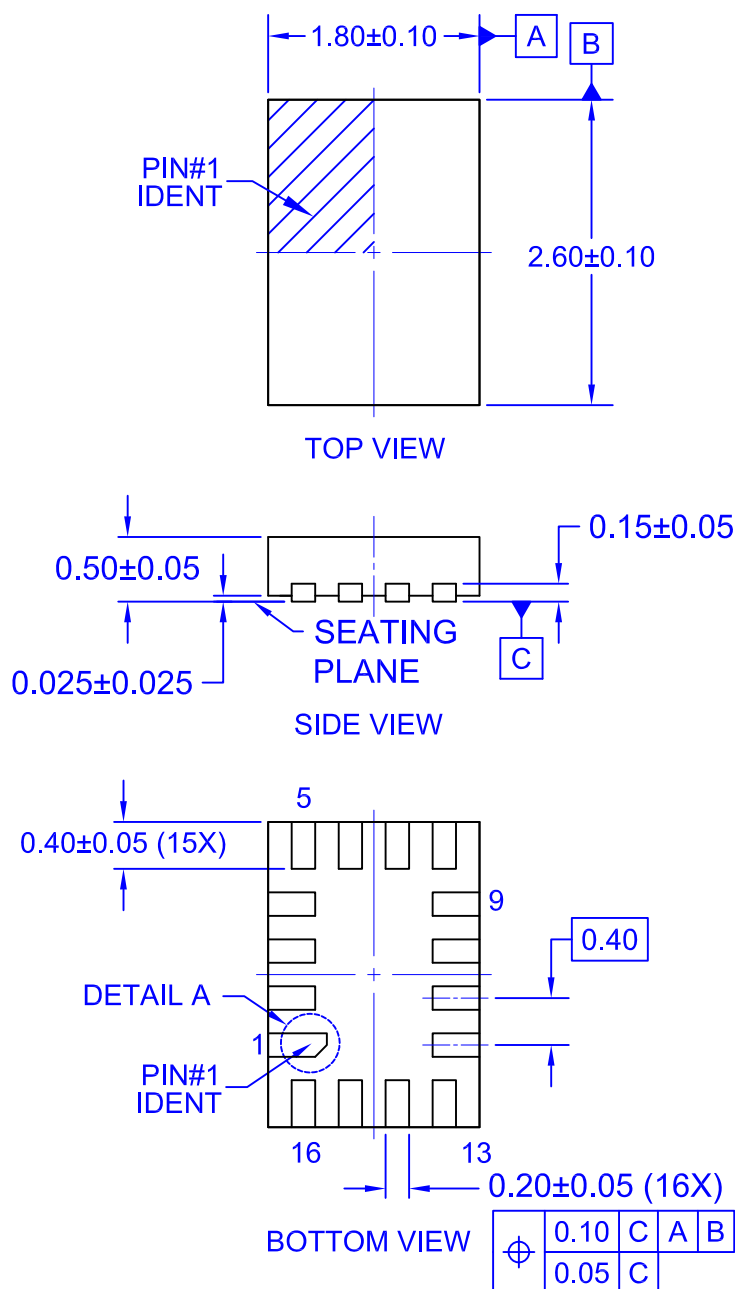
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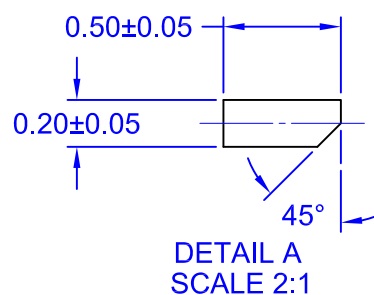
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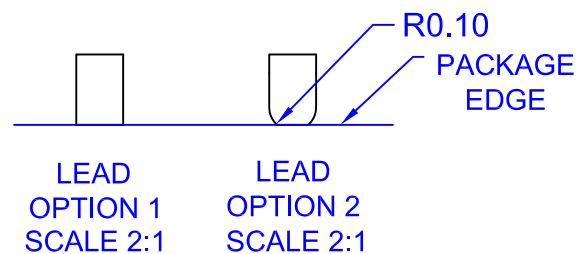




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